Electronic Version
Stylesheet Version v1.1.1

Description

[METHOD OF FORMING DUAL-IMPLANTED GATE AND STRUCTURE FORMED BY THE SAME]

Cross Reference to Related Applications

[0001] This application is a divisional application of prior US application No. 10/064,372, filed on July 08, 2002.

Background of Invention

[0002] Field of Invention

[0003] The present invention relates to a method of forming a semiconductor device and a structure formed by the same. More particularly, the present invention relates to a method of forming a dual-implanted gate and a structure formed by the same.

[0004] Description of Related Art

[0005] At present, the gate of most semiconductor devices has a stack structure that includes a doped polysilicon layer and a metallic layer or a metal silicide layer. To manufacture a

semiconductor device having both n-doped and p-doped polysilicon gates, the so-called "dual-implanted gate", polysilicon material is first deposited over a substrate. An ion implantation is carried out to implant ions into the substrate such that n-type dopants are implanted into NMOS region and p-type dopants are implanted into PMOS region. Thereafter, a layer of tungsten or tungsten silicide (WSi_x) is formed over the doped polysilicon layer. Finally, an etching operation is conducted to pattern out a dual-implanted gate structure.

[0006] However, the deposition of tungsten or tungsten silicide over the polysilicon layer often leads to an out-diffusion of dopant ions. This is because the grain boundary of the tungsten or tungsten silicide layer is relatively large. Hence, the n-type or p-type ions within the doped polysilicon layer can easily diffuse through the tungsten or tungsten silicide layer into another polysilicon layer. Under such circumstances, the concentration of dopants within the polysilicon layer is likely to drop, leading to a degradation of device performance.

[0007] In addition, if a tungsten layer is formed over the polysilicon layer, difference in material properties between tungsten and polysilicon may lead to the production of gates

having an irregular shape after patterning through an etching operation. Similarly, due to a difference in material properties between tungsten and polysilicon, the tungsten layer may peel off from the doped polysilicon layer after a subsequent thermal processing operation.

SUMMARY OF INVENTION

[0008] Accordingly, one object of the present invention is to provide a method of forming a dual-implanted gate capable of preventing doped ions having different electrical states from cross diffusing through an overhead metallic layer.

[0009] A second object of this invention is to provide a method of forming a dual-implanted gate capable of preventing any change in concentration of doped ions inside a doped polysilicon layer.

[0010] A third object of this invention is to provide a method of forming a dual-implanted gate and a structure formed by the same, which is capable of preventing the degradation of device performance.

[0011] A fourth object of this invention is to provide a method of forming a dual-implanted gate and a structure formed by the same, which is capable of preventing the formation of gates having an irregular shape.

[0012] A fifth object of this invention is to provide a method of

forming a dual-implanted gate and a structure formed by the same, which is capable of preventing an overhead metallic layer from peeling off a doped polysilicon layer.

[0013] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a method of forming a dual-implanted gate. The method includes the following steps. First, a substrate having a gate oxide layer thereon is provided. A polysilicon layer, a sacrificial layer and a mask layer are sequentially formed over the substrate. The polysilicon layer, the sacrificial layer and the mask layer are patterned to form a first structure for forming an N-type gate and a second structure for forming a P-type gate. A dielectric layer is formed over the substrate covering the first and the second structure. The dielectric layer is planarized to expose the upper surface of the mask layer in the first and the second structure. The mask layer is removed to form a plurality of trenches. The first and the second structure are implanted using ions having different electrical states. The sacrificial layer is removed. Thereafter, a barrier layer is formed over the substrate. A metallic layer is formed over the substrate completely filling the trenches. The metallic layer is pla-

narized to remove excess metal outside the trench. The exposed barrier layer is removed and then the dielectric layer is removed to form a plurality of gate structures. Finally, spacers may form on the sidewalls of the gate structures.

[0014] In this invention, a barrier layer is formed over the doped polysilicon layer before forming the metallic layer. Thus, dopants having different electrical states within the doped polysilicon layer are prevented from cross diffusing with the overhead metallic layer. Hence, changes in dopant concentration within the doped polysilicon layer and the peeling of the metallic layer away from the doped polysilicon layer are prevented. Ultimately, device performance can be maintained. Furthermore, by enclosing the sidewall of the metallic layer with a barrier layer, the formation of irregular-shaped gates due to a difference in material properties between the metallic layer and the polysilicon layer is largely avoided.

[0015] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a dual-implanted gate. The dual-implanted gate includes a stack structure and a spacer on a substrate. The stack structure

includes a polysilicon bottom layer, a barrier layer and a metallic layer, the metallic layer being surrounding by the barrier layer. The spacer is formed on the stack layer over the substrate and the stack structure is enclosing by the spacer.

[0016] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a dual-implanted gate. The dual-implanted gate includes a plurality of stack structures and a plurality of corresponding spacers. The stack structure includes a polysilicon bottom layer, a barrier layer and a metallic layer, the metallic layer being surrounding by the barrier layer. The spacer is formed on the stack layers over the substrate and each of the stack structure is enclosed by the corresponding one of the spacers.

[0017] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

Brief Description of Drawings

[0018] The accompanying drawings are included to provide a further understanding of the invention, and are incorpo-

rated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0019] Figs. 1A to 1J are schematic cross-sectional views showing the progression of steps for producing a dual-implanted gate according to one preferred embodiment of this invention.

Detailed Description

[0020] Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

[0021] Figs. 1A to 1J are schematic cross-sectional views showing the progression of steps for producing a dual-implanted gate according to one preferred embodiment of this invention. As shown in Fig. 1A, a substrate 100 having a gate oxide layer 102 thereon is provided. A plurality of stack structures 110 each having a polysilicon layer 104, a sacrificial (SAC) layer 106 and a mask layer 108 is formed over the gate oxide layer 102. The sacrificial layer

106 can be an oxide layer and the mask layer can be a polysilicon layer or other material having a high etching selectivity relative to a subsequently formed dielectric layer, for example. The stack structure 110 is formed, for example, by a series of deposition processes to form a polysilicon layer, a sacrificial layer and a mask layer sequentially over the substrate 100. Thereafter, the polysilicon layer, the sacrificial layer and the mask layer are patterned to form a first structure 110a for implanting p-type dopants and a second structure 110b for implanting n-type dopants.

[0022] As shown in Fig. 1B, a dielectric layer is formed over the substrate 100 covering the stack structure 110. The dielectric layer 112 can be a silicon nitride layer, silicon oxide layer or other material having a high etching selectivity ratio relative to the mask layer 108, for example.

[0023] As shown in Fig. 1C, the dielectric layer 112 is planarized to expose the upper surface of the mask layer 108 within the stack structures 110, for example, by conducting a chemical-mechanical polishing (CMP) operation.

[0024] As shown in Fig. 1D, the mask layer 108 is removed to form a plurality of trenches 114. The mask layer 108 can be removed by dry etching, for example.

[0025] As shown in Fig. 1E, a patterned photoresist layer 116 is formed over the substrate 100 so that the second structure 110b for receiving n-type dopants is covered while the first structure 110a for receiving p-type dopants is exposed. Thereafter, an ion implantation 118 is carried out implanting p-type ions into first structure 110a so that the polysilicon layer 104 is converted into a p-doped polysilicon layer 104a. The p-type dopants include boron or boron difluoride (BF_2) ions for example.

[0026] As shown in Fig. 1F, the photoresist layer 116 is removed. Another patterned photoresist layer 120 is formed over the substrate 100 such that the first structure 110a is covered while the second structure 110b for receiving n-type dopants is exposed. Thereafter, another ion implantation 122 is carried out implanting n-type ions into the second structure 110b so that the polysilicon layer 104 is converted into an n-doped polysilicon layer 104b. The n-type dopants include phosphorus or arsenic, for example.

[0027] As shown in Fig. 1G, the photoresist layer 120 is removed. Thereafter, the sacrificial layer 106 is removed. A barrier layer 124 is formed over the substrate 100. The barrier layer 124 can be a composite layer such as a titanium/titanium nitride (Ti/TiN) layer. An annealing operation such

as a rapid thermal process (RTP) may be conducted to lower the contact resistance with a subsequently formed overhead metallic layer. A metallic layer 126 is formed over the substrate 100 completely filling the trenches 114. The metallic layer can be a tungsten layer, for example. The barrier layer 124 between the metallic layer 126 and the doped polysilicon layers 104a and 104b prevents n-type or p-type ions from diffusing into another polysilicon layer through the metallic layer 126. In other words, the barrier layer 124 is an effective barrier to the out-diffusion of dopants.

[0028] As shown in Fig. 1H, the metallic layer 126 is planarized using the barrier layer 124 as an etching end point. This removes the metallic layer 126 above the trenches 114. The metallic layer 126 is planarized by chemical-mechanical polishing, for example.

[0029] As shown in Fig. 1I, the exposed barrier layer 124 is removed so that the upper surface of the dielectric layer 112 is exposed. Similarly, the barrier layer 124 may be removed by chemical-mechanical polishing.

[0030] As shown in Fig. 1J, the dielectric layer 112 is removed to form a p-doped gate structure 128a and an n-doped gate structure 128b. Finally, spacers 130 are formed on the

sidewalls of the gate structures 128a and 128b. The spacers 130 can be a silicon nitride layer, for example.

[0031] In conclusion, major aspects of this invention includes: 1. A barrier layer is formed over the doped polysilicon layer before depositing metallic material to form the metallic layer. Hence, dopants having different electrical properties are prevented from out-diffusing from the doped polysilicon layer through the metallic layer and vice versa. 2. Since the barrier layer between the doped polysilicon layer and the metallic layer prevents any cross-diffusion of n-type or p-type ions, dopant concentration within various doped polysilicon layers can be maintained. 3. Without out-diffusion of dopants, device performance is reliable. 4. By enclosing the sidewall of the metallic layer with a barrier layer, irregularity in gate profile due to a difference in material properties between the metallic layer and the polysilicon layer is prevented. 5. Because the metallic layer and the doped polysilicon layer are separated from each other by a barrier layer, the metallic layer is prevented from peeling away from an underlying doped polysilicon layer.

[0032] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure

of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.